

## ABSTRACT:

A processor executes image processing under control of a clock facility, such that a sequence of  $C$  effective clock cycles will effect a processing operation of a predetermined amount of image information. In particular, the processor has programming means for implementing programmable stall clock cycles interspersed between the effective clock cycles for implementing a programmable slowdown factor  $S$ , such that a modified number of  $C*S$  overall clock cycles will effect processing of the predetermined amount of image information.

FIGURE: 2